BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,738	01/04/2002	Paul Magliocco	A-70697/ENB/WEN	1137

7590 08/04/2004

FLEHR HOHBACH TEST ALBRITTON & HERBERT LLP
Suite 3400
Four Embarcadero Center
San Francisco, CA 94111-4187

EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,738	MAGLIOCCO, PAUL	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/12/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-23 are presented for examination.

Double Patenting Rejections

2. Claim 1 of patent US 6,754,868 B2 contain every element of claim 1 of the instant application and as such anticipate claim 1 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus)." ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

3. Claim 1 of the instant application is anticipated by patent US 6,754,868 claim 1 in that claim 1 of the patent US 6,754,868 contains all the limitations of claim 1 of the instant application. Claim 1 of the instant application therefore is not patently distinct from the earlier patent claim and as such is unpatentable for obvious-type double patenting.

4. The obviousness-type double patenting rejection is a judicially established doctrine based upon public policy and is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinct from claims in a first patent. *In re Vogel*, 164 USPQ 619 (CCPA 1970). A timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 C.F.R. § 1.78(d).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 4-7, 10-17, 20-23 are rejected under 35 U.S.C. § 102 (e) as being anticipated by Bristow et al. (US Patent 6,754,868 B2 hereafter referred to as Bristow).

As per claim 1:

Bristow discloses an apparatus for testing a device under test (DUT) having a plurality of pins [fig.3, col. 9, lines 7-8] the apparatus comprising:

- a clock having a clock cycle [col. 9, line 21];
- plurality of pin electronics channels (PEs) capable of coupling to the plurality of pins on the DUT [col. 9, lines 11-12];

- a plurality of timing and format circuits (T/Fs) each capable of mapping a signal to one of the plurality of PEs [col. 9, lines 13-14];
- a pattern memory capable of storing a number of bits for testing the DUT, the pattern memory having a plurality of outputs capable of outputting the bits to test the DUT [col. 9, lines 20-21];
- a pattern scrambler coupled between the plurality of outputs and the plurality of T/Fs, the pattern scrambler capable of being programmed to couple bits from one or more of the plurality of outputs to one or more of the plurality of T/Fs, to provide a test pattern to the DUT having a width of from 1 bit wide to a width equal to the number of the plurality of PEs [col. 9, lines 17-19].

As per claim 4:

Bristow discloses the pattern scrambler is capable of coupling bits from any one of the plurality of outputs to any one of the plurality of PEs and wherein the pattern scrambler is capable of changing bits coupled to one or more of the plurality of PEs on a cycle-by-cycle basis for each clock cycle of the test system [col. 3, lines 64-66].

As per claim 5:

Bristow discloses the pattern memory is capable of being operated to simultaneously provide a logic vector memory (LVM) for storing logic vectors of a number of bits and having a width and a depth, and a scan memory for storing scan vectors of a number of bits and having a width and a depth [fig.5, col. 6, lines 60-68].

As per claim 6:

Bristow discloses logic vectors stored in the LVM and the scan vectors stored in the scan memory comprise different widths [col.7, lines 1-6, col. 9, lines 39-42].

As per claim 7:

Bristow discloses a pattern generator for testing at least one device under test (DUT) having a plurality of pins [col.9, lines 9-10], the pattern generator comprising:

- a pattern memory capable of storing a number of bits for testing the DUT, the pattern memory having a plurality of outputs capable of outputting the bits to test the DUT [col. 9, lines 20-21];
- a pattern scrambler coupled between the plurality of outputs and the plurality of pins on the DUT, the

pattern scrambler capable of being programmed to couple bits from one or more of the plurality of pins on the DUT, to provide a test pattern to the DUT having a width of from 1 bit wide to a width equal to the number of the plurality of outputs [col. 9, lines 17-19].

As per claims 10-11:

Bristow discloses the pattern scrambler is capable of being programmed to couple bits from each one of the plurality of outputs to one or more of the plurality of pins on one or more DUTs on a cycle-by-cycle basis for each clock cycle of the test system [col. 3, lines 64-66].

As per claim 12:

Bristow discloses the pattern memory is capable of being operated to simultaneously provide a logic vector memory (LVM) for storing logic vectors of a number of bits and having a width and a depth, and a scan memory for storing scan vectors of a number of bits and having a width and a depth [fig.5, col. 6, lines 60-68].

As per claim 13:

Bristow discloses logic vectors stored in the LVM and the scan vectors stored in the scan memory comprise different widths [col.7, lines 1-6, col. 9, lines 39-42].

As per claim 14:

Bristow discloses the test system further comprising a clock having a clock cycle, and wherein the logic vectors delivered from the LVM and the scan vectors delivered from the scan memory can be changed by the pattern scrambler on a cycle-by-cycle basis for each clock cycle of the test system[col. 3, lines 64-66].

As per claim 15:

Bristow discloses the scrambler is capable of being programmed to couple a data bit of the plurality of outputs, output n, to one or more of the plurality of pins on the DUT, while strobe and I/O control bits of output n are coupled to one or more of the plurality of pins on the DUT, different from the one or more of the plurality of pins on the DUT to which the data bit is coupled [col. 6, lines 31-45].

As per claim 16:

Bristow discloses the test system further comprising a clock having a clock having a clock cycle, and wherein the pattern scrambler is capable of switching bits from any one of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle [col. 6, lines 45-45, col.9, lines 21-27].

As per claim 17:

Bristow discloses a method for testing a device under test (DUT) using a test system including a pattern memory having a plurality of outputs equal to n, and a pattern scrambler coupled between the 0plurality of outputs and a plurality of pins on the DUT [abstract, fig.3, col.10, lines 17-20], the method comprising:

- storing a number of bits for testing the DUT in the pattern memory [col. 7, lines 7-10];
- programming the pattern scrambler to output bits from one or more of the plurality of outputs to one or more of the plurality of pins on the DUT, and to provide a test pattern to the DUT having a width of from 1 to n bits [col. 6, lines 31-48].

As per claims 20, 21, 22:

Due to the similarity of claims 20-22 to claims 11-13; therefore, these claims are also rejected under the same rationale applied against claims 11-13. **In addition, all of the limitations have been noted in the rejection as per claims** 11-13.

As per claim 23:

Bristow discloses the test system further comprising a clock having a clock having a clock cycle, and wherein the pattern scrambler is capable of switching bits from any one of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle [col. 6, lines 45-45, col.9, lines 21-27].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-3, 8-9, 18-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable Bristow et al. (US Patent 6,754,868 B2 hereafter referred to as Bristow) in view of Fujisaki (US Patent 5,852,618).

As per claims 2-3:

Bristow further teaches:

- pattern generation and scrambler [fig. 3, col. 5, lines 45-55];

- DUT signaling (i.e., cycle by cycle) [col. 7, lines 7-45];

- memory look up [col. 7, line 2].

Bristow does not disclose:

- test pattern having a depth of from n x m bits.

However, Bristow does disclose capabilities of:

- scrambler 1 through n, coupled at least two output in supporting the DUT clock cycle [col. 6, lines 40-49].

- test DUT [col. 5, lines 10-14].

In addition, Fujisaki does explicitly disclose:

- Multiple bit test pattern generator for testing memory with a multi-bit data width [abstract, col. 1, lines 8-10] comprising:

- a multi-bit data width [col. 1, lines 45-46];

- data having a 1/n width of data bit [col. 5, lines 8-9];

- test pattern with 72 bit data width [col. 2, lines 65-67].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to include the multi bit data width and its test pattern with 72 bit data width of Fujisake into the method and apparatus of Bristow. A person of ordinary skill in the art would have been motivated to make the modification because this multi bit width arrangement does enhance the

testing of the DUT. By utilizing this approach, the DUT test can perform with high reliability and throughput.

As per claims 8-9, 18-19:

Due to the similarity of claims 8-9, 18-19 to claims 2-3; therefore, these claims are also rejected under the same rationale applied against claims 2-3. **In addition, all of the limitations have been noted in the rejection as per claims 2-3.**

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
7/29/04